

REMARKS

Claims 1, 16-18, 20 and 21 were examined. All claims were rejected. In response to the above-identified Office Action, Applicants amend claims 1 and 18, cancel claims 17 and 21, and add new claims 22-27. Reconsideration of the rejected claims in light of the aforementioned amendments and the following remarks is requested.

I. Claims Rejected Under 35 U.S.C. § 102(e)

The Examiner rejected claims 1, 16, 18 and 20 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,654,242 issued to Komatsu ("*Komatsu*"). For the reasons discussed below, Applicants believe *Komatsu* fails to anticipate the amended claims.

As to claim 1, that claim recites a circuit device comprising, *inter alia*, a first metal gate of tantalum. *Komatsu* teaches only gates of tungsten silicide (WSi_x) and "other known high-melting silicides." However, it does not teach or suggest a first metal gate of tantalum. For at least this reason, Applicants submit that *Komatsu* does not anticipate claim 1, and respectfully request that the Examiner withdraw the rejection thereof.

As to claim 16, that claim depends upon claim 1, and is patentable for at least the reasons discussed in support of that claim. Applicants ask the Examiner to withdraw the rejection of claim 16.

As to claim 18, that claim has been amended to incorporate all the limitations of claim 21, which the Examiner noted to contain allowable material. As amended, Applicants believe that the claim is allowable, and ask the Examiner to withdraw this rejection.

II. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claim 17 under 35 U.S.C. § 103(a) as unpatentable over *Komatsu (supra.)* Applicants have canceled this claim, so its rejection is moot.

III. New Claims

New claim 22 recites a circuit device comprising a first transistor with a tantalum gate and a second, complementary transistor with a tantalum nitride gate, formed on a semiconductor substrate. Support for this claim is at Specification, p. 12, line 12 through p. 13, line 9 and Figure 5. The references of record fail to teach at least the tantalum and

tantalum nitride gates, and so Applicants respectfully submit that the claim is allowable over those references.

New claim 23 recites a circuit device comprising a first transistor with a molybdenum silicide gate and a second, complementary transistor with a molybdenum nitride gate, formed on a semiconductor substrate. Support for this claim is at Specification, p. 11, line 20 through p. 12, line 11 and Figure 4. The references of record fail to teach at least a complementary transistor structure containing both molybdenum silicide and molybdenum nitride gates, and so Applicants respectfully submit that the claim is allowable over those references.

New claim 24 recites a circuit device comprising a first transistor with a first gate electrode and a second, complementary transistor with a second gate electrode, wherein the first gate is composed of a gate material, and the second metal gate is composed of a nitride of the gate material. Support for this claim is at Specification, p. 11, lines 11-19. The references of record fail to teach at least the use of a gate material *and* a nitride of *the same gate material* for metal gate electrodes of complementary transistors on a semiconductor substrate, and so Applicants respectfully submit that the claim is allowable over those references.

New claim 25 depends upon new claim 24, and claims material disclosed in the specification at p. 11, lines 11-19.

New claim 26 recites a circuit device comprising a first transistor with a first gate electrode and a second, complementary transistor with a second gate electrode, wherein the first gate is composed of a nitride of a gate material, and the second gate is composed of a silicide of the gate material. Support for this claim is at Specification, p. 11, line 20 through p. 12, line 11. The references of record fail to teach at least the use of *both* a nitride of a gate material *and* a silicide of *the same gate material* for metal gate electrodes of complementary transistors on a semiconductor substrate, and so Applicants respectfully submit that the claim is allowable over those references.

New claim 27 depends upon new claim 26, and claims material disclosed in the specification at p. 11, lines 1-11.

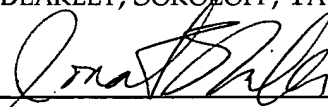
IV. Allowable Material

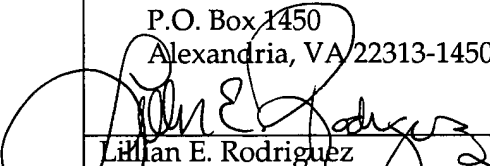
Applicants note with appreciation that the Examiner determined claim 21 to contain allowable material. The limitations of claim 21 have been incorporated into its base claim, claim 18, and favorable consideration of that claim is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1, 16, 18, 20 and 22-27, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Dated: 1/4/05, 2005 Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP


Jonathan S. Miller, Reg. No. 48,534

<p>12400 Wilshire Boulevard Seventh Floor Los Angeles, California 90025 (310) 207-3800</p>	<p style="text-align: center;"><u>CERTIFICATE OF MAILING</u></p> <p>I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:</p> <p style="text-align: center;">Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450</p> <p> Lillian E. Rodriguez</p> <p style="text-align: right;">January 4, 2005</p>
---	---